a first comparator having a first input coupled for receiving the control signal, a second input coupled for receiving the first reference signal, and an output coupled to the first input of the memory circuit; and

a second comparator having a first input coupled for receiving the control signal, a second input coupled for receiving a second reference signal, and an output coupled to a second input of the memory circuit.

3. The power conversion integrated circuit of claim **2**, further including a resistor divider network for generating the first reference signal at a first output and the second reference signal at a second output.

4. The power conversion integrated circuit of claim **3**, wherein the resistor divider network includes:

a first resistor having first and second terminals, the first terminal of the first resistor coupled to a first power supply conductor;

a second resistor having first and second terminals, the first terminal of the second resistor coupled to the second terminal of the first resistor and serving as the first output of the resistor divider network; and

a third resistor having first and second terminals, the first terminal of the third resistor coupled to the second terminal of the second resistor and serving as the second output of the resistor divider network, and the second terminal of the third resistor coupled to a second power supply conductor.

5. The power conversion integrated circuit of claim **4**, further including a pulse filter having an input coupled to the output of the second comparator and an output coupled to the second input of the memory circuit.

6. The power conversion integrated circuit of claim **1**, wherein the memory circuit has at least one storage element for storing an operating mode of the power conversion integrated circuit.

7. The power conversion integrated circuit of claim **1**, further including a reset circuit having an input coupled to a logic under voltage signal and an output coupled to the control signal.

8. A semiconductor chip having at least four external electrical connections, comprising:

an internal regulator; a state circuit having an output coupled to a control input of the internal regulator;

a first electrical connection terminal for coupling an external ground reference to an internal ground reference of the internal regulator;

a second electrical connection terminal for providing a pulse-width modulated output signal from an output of the internal regulator;

a third electrical connection terminal coupled for receiving a feedback signal at an input of the internal regulator to control the pulse-width modulated output signal; and

a fourth electrical connection terminal coupled for receiving a control signal which is applied to the state circuit to set a mode of operation of the internal regulator.

9. The semiconductor chip of claim **8**, further comprising a fifth electrical connection terminal coupled for receiving a bias voltage which is applied to the state circuit and to the internal regulator.

10. A programmable power supply, comprising:

a transformer receiving a rectified signal at a primary side of the transformer;

a state circuit having an input and an output for setting a mode of operation of the programmable power supply, wherein the state circuit includes,

a comparator circuit having a first input coupled to the input of the state circuit for receiving a control signal and a second input coupled for receiving a first reference signal, and

a memory circuit having a first input coupled to an output of the comparator for setting an output state of the memory circuit according to a value of the control signal where the output state of the memory circuit controls the mode of operation;

a control circuit coupled for receiving the output state of the memory circuit and wherein the control circuit is responsive to a feedback signal for providing a pulse-width modulated control signal; and

a transistor having a control terminal for receiving the pulse-width modulated control signal, a first conduction terminal coupled to the primary side of the transformer, and a second conduction terminal coupled to ground.

11. The programmable power supply of claim **10**, wherein the comparator circuit includes:

a first comparator having a first input coupled for receiving the control signal, a second input coupled for receiving the first reference signal, and an output coupled to the first input of the memory circuit; and

a second comparator having a first input coupled for receiving the control signal, a second input coupled for receiving a second reference signal, and an output coupled to a second input of the memory circuit.

12. The programmable power supply of claim **10**, further including a resistor divider network for generating a first reference signal at a first output and a second reference signal at a second output.

13. The programmable power supply of claim **12**, wherein the resistor divider network includes:

a first resistor having first and second terminals, the first terminal of the first resistor coupled to a first power supply conductor;

a second resistor having first and second terminals, the first terminal of the second resistor coupled to the second terminal of the first resistor and serving as the first output of the resistor divider network; and

a third resistor having first and second terminals, the first terminal of the third resistor coupled to the second terminal of the second resistor and serving as the second output of the resistor divider network, and the second terminal of the third resistor coupled to a second power supply conductor.

14. A method for controlling a mode of operation of a power converter, comprising the steps of:

controlling a pulse-width modulated output signal of the power converter in response to a feedback signal; and

setting a memory state according to a comparison between a control signal and a first reference signal where the memory state controls the mode of operation of the power converter.

15. The method of claim **14**, further comprising the steps of:

monitoring a signal at an input pin; and

maintaining a same operating state when the input pin receives a voltage about midway between an operating potential and a ground reference.

16. The method of claim **14**, further comprising the steps of requesting an on-operating state when a power supply is off and an input pin receives a voltage greater than a first reference voltage.

17. The method of claim 14, further comprising the steps of requesting a toggle condition when a power supply is on and an input pin receives a voltage greater than a first reference voltage.

18. The method of claim 15, further comprising the steps of requesting that an output state be toggled when a power supply is on and an input pin receives a voltage less than a second reference voltage.

19. The method of claim 14, further comprising the step of operating in an off-operating state when a brown-out

occurs that includes receiving a signal that is proportional to a line voltage that is less than a second reference voltage.

20. The method of claim **14**, further comprising the step of operating in an off-operating state when a black-out occurs that includes receiving a signal that is proportional to a line voltage that is less than a second reference voltage.

* * * * *